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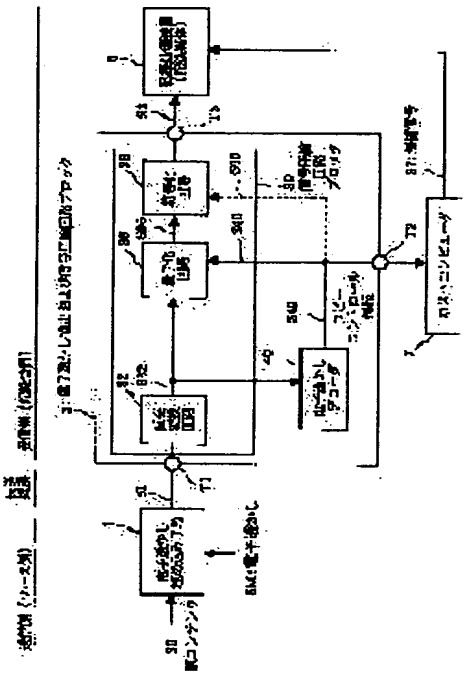
(54) ENCODING CIRCUIT AND SIGNAL PROCESSOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an encoding circuit that is effective against falsification.
SOLUTION: A digital watermark imbed means 1 imbeds a digital watermark including copy control information(CC information) to original contents S0. An orthogonal transformation circuit 32, a quantization circuit 36, an encoding circuit 38 and a digital watermark decoder 40 are integrated in order to make impossible an external access to a digital watermark decode and a signal compression circuit block 3 acting as the encoding circuit. The orthogonal transformation circuit 32 applies orthogonal transformation to digital watermark imbed information S1 into a sub-band signal, and the digital watermark decoder 40 detects the CC information S40. The quantization circuit 36 quantizes an orthogonal transformation processing signal S32 only when a copy of the CC information is permitted and the coding circuit 38 encodes a quantized signal S36 only when the copy of the CC information is permitted. The quantization circuit 36 or the encoding circuit 38 outputs invalid data when the copy of the CC information is inhibited so as to output a meaningless copy on the occurrence of falsification.



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